
*128MB to 16GB*
*IDE Flash Drive*

SimpleTech®
www.simpletech.com

# SLFLD25-xxx(M/G)M1U(I)

ATA-5 Compatible

Supports True-IDE Interfaces

Capacities from 128MB to 16GB

Form Factors:

- 2.5-inch Ruggedized Enclosure with 44-Pin IDE Connector

Endurance Guarantee of 2,000,000 Write/Erase Cycles

Configures to Master or Slave IDE Device

5V or 3.3V Power Supply

Completely Solid-State (No Moving Parts)

Available in Commercial and Industrial Operating Temperature Ranges

7-Byte Detection, 4-Byte Correction ECC Engine

RoHS-6 Compliant Lead-Free

5-Year Warranty

## General Description

The SimpleTech SLFLD25-xxx(M/G)M1U(I) are IDE flash drives with 128MB to 16GB of nonvolatile storage. The drives have 44-pin IDE connector and a ruggedized 2.5-inch form-factor enclosure. The drives use a flash memory controller that provides a fully compatible IDE interface for the flash memory.

SimpleTech OEM IDE flash drives are the product of choice in applications requiring high reliability and high tolerance to shock, vibration, humidity, altitude, and temperature. Because there are no moving parts to service or maintain, IDE flash drives are reliable alternatives to mechanical hard disk drives for high availability and mission critical applications.

While the inherent ruggedness and reliability of solid-state storage relative to rotating hard drives is intuitive, new applications for OEM IDE flash drives are emerging due to the low cost per usable megabyte. Most applications using embedded operating systems such as VxWorks™, Windows XP/embedded™, and Linux™ don't have multi-gigabyte data storage requirements, and therefore a cost savings can be realized when using this robust media.

## Ordering Information

### IDE Flash Drive

| Part Number* | IDE Form Factor | Capacity |
|---|---|---|
| SLFLD25-128MM1U(I) | 2.5-inch/44-pin | 128 Mbytes |
| SLFLD25-256MM1U(I) | 2.5-inch/44-pin | 256 Mbytes |
| SLFLD25-512MM1U(I) | 2.5-inch/44-pin | 512 Mbytes |
| SLFLD25-1GM1U(I) | 2.5-inch/44-pin | 1 GByte |
| SLFLD25-2GM1U(I) | 2.5-inch/44-pin | 2 GBytes |
| SLFLD25-3GM1U(I) | 2.5-inch/44-pin | 3 GBytes |
| SLFLD25-4GM1U(I) | 2.5-inch/44-pin | 4 GBytes |
| SLFLD25-5GM1U(I) | 2.5-inch/44-pin | 5 GBytes |
| SLFLD25-6GM1U(I) | 2.5-inch/44-pin | 6 GBytes |
| SLFLD25-7GM1U(I) | 2.5-inch/44-pin | 7 GBytes |
| SLFLD25-8GM1U(I) | 2.5-inch/44-pin | 8 GBytes |
| SLFLD25-10GM1U(I) | 2.5-inch/44-pin | 10 GBytes |
| SLFLD25-12GM1U(I) | 2.5-inch/44-pin | 12 GBytes |
| SLFLD25-14GM1U(I) | 2.5-inch/44-pin | 14 GBytes |
| SLFLD25-16GM1U(I) | 2.5-inch/44-pin | 16 GBytes |

* Custom capacities available

**Legend:**

- **(I)** = industrial operating temperature range option.
- **Part numbers without (I)** = commercial operating temperature range option.
- **(M/G)** indicates if preceeding capacity (xxx) is in Megabytes (M) or Gigabytes (G).

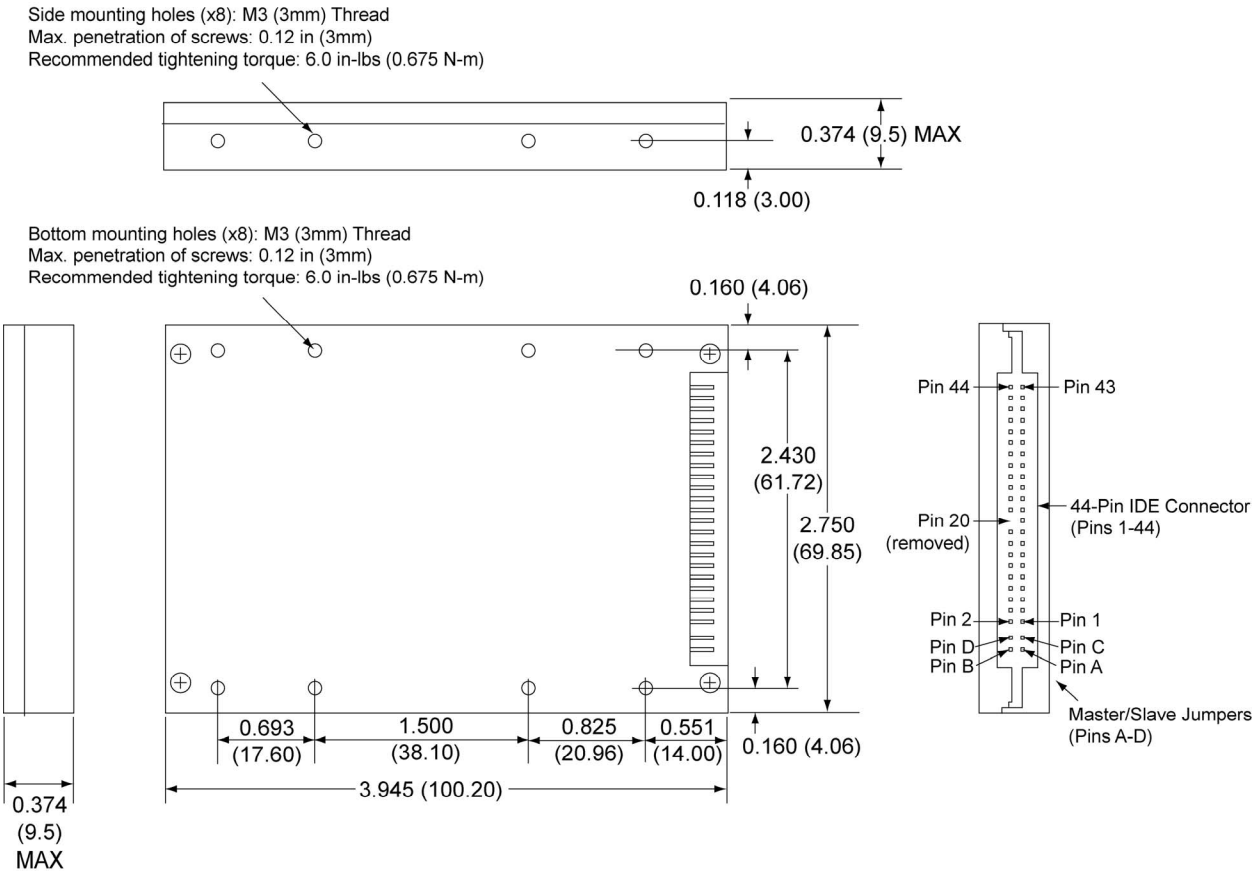
## Table of Contents

## Package Dimensions, Mounting Hole Locations, Jumper Locations and Pin Locations

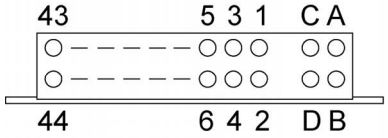
### Standard 2.5-Inch Form Factor

| Parameter | Value |
|---|---|
| Length | 3.945 ±. 0.005 in (100.20 ± 0.127 mm) |
| Width | 2.750 ± 0.005 in (69.85 ± 0.127 mm) |
| Height | 0.374 in max (9.5 mm max) |

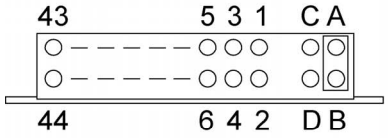
Units: inches (mm)



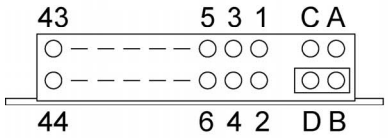
## Jumper Settings




If all pins A, B, C, and D are open, the drive is in master mode.




If pin A is jumpered to pin B, the drive is in slave mode.




If pin B is jumpered to pin D, the drive mode is determined by the -CSEL signal (Pin 28).

NOTE: In multiple drive configuration, it may become necessary to establish master drive and slave drive. This can be done by booting the PC and using IDE HDD Auto Detection available in CMOS setup.

## Pin Assignments

| Pin Number | Signal Name | Pin Type | Pin Number | Signal Name | Pin Type |
|---|---|---|---|---|---|
| 1 | -RESET | I | 23 | -IOWR | I |
| 2 | GND | Ground | 24 | GND | Ground |
| 3 | D07 | I/O | 25 | -IORD | I |
| 4 | D08 | I/O | 26 | GND | Ground |
| 5 | D06 | I/O | 27 | -IORDY | O |
| 6 | D09 | I/O | 28 | -CSEL | I |
| 7 | D05 | I/O | 29 | -DMACK | I |
| 8 | D10 | I/O | 30 | GND | Ground |
| 9 | D04 | I/O | 31 | INTRQ (-IREQ) | O |
| 10 | D11 | I/O | 32 | -IOIS16 | O |
| 11 | D03 | I/O | 33 | A1 | I |
| 12 | D12 | I/O | 34 | -PDIAG | I/O |
| 13 | D02 | I/O | 35 | A0 | I |
| 14 | D13 | I/O | 36 | A2 | I |
| 15 | D01 | I/O | 37 | -CE1 | I |
| 16 | D14 | I/O | 38 | -CE2 | I |
| 17 | D00 | I/O | 39 | -DASP | I/O |
| 18 | D15 | I/O | 40 | GND | Ground |
| 19 | GND | Ground | 41 | VCC | Power |
| 20 | Key | Key | 42 | VCC | Power |
| 21 | DMARQ | O | 43 | GND | Ground |
| 22 | GND | Ground | 44 | NC | No Connect |

## Signal Descriptions

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| -DASP | I/O | 39 | This input/output is the Disk Active/Slave Present signal in the Master/ Slave handshake protocol. |
| D15-D00 | I/O | 18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17 | All Task File operations occur in byte mode on the low order bus D00-D07 while all data transfers are 16 bit using D00-D15. |
| -IOWR | I | 23 | The I/O Write strobe pulse is used to clock I/O data on the drive Data bus into the Drive controller registers when the Drive is configured to use the I/O interface. The clocking will occur on the negative to positive edge of the signal (trailing edge). |
| -IORD | I | 25 | This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Drive. |
| INTRQ (-IREQ) | O | 31 | Signal is the active high Interrupt Request to the host. |
| A2-A0 | I | 35, 33, 36 | A[2:0] are used to select the one of eight registers in the Task File. |
| -CE1, -CE2 | I | 37, 38 | -CS1 is the chip select for the task file registers while -CS2 is used to select the Alternate Status Register and the Device Control Register. |
| -CSEL | I | 28 | This internally pulled up signal is used to configure this device as a Master or a Slave. When the pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave |
| -IOIS16 | O | 32 | Not used. |
| -PDIAG | I/O | 34 | This input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol. |
| DMARQ | O | 21 | This signal is asserted by the device when it is ready to transfer data to/ from the host. Data direction is controlled by -IORD and -IOWR. This signal is used in a handshake manner with –DMACK. |
| -DMACK | I | 29 | This input signal is used by host in response to DMARQ to initiate DMA transfers. |
| -IORDY | O | 27 | Not used, and pulled up to VCC through a 4.7K ohm resistor. |
| -RESET | I | 1 | This input pin is the active low hardware reset from the host. |
| VCC | — | 41, 42 | Power. |
| GND | — | 2, 19, 22, 24, 26, 30, 40, 43 | Ground. |
| Key | — | 20 | This pin is keyed to ensure cable is connected with the proper orientation. |

## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin w.r.t. Vss | Vin, Vout | -0.5 to VCC +0.5 | V |
| Storage temperature range | Tstg | -65 to +150 | °C |

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Commercial operating temperature | Ta | 0 | 25 | 70 | °C |
| Industrial operating temperature | Ta | -40 | — | 85 | °C |
| VCC voltage | VCC | 4.75<br>3.18 | 5.0<br>3.3 | 5.25<br>3.465 | V |

## Performance

| Parameter | Value |
|---|---|
| Data transfer rate to/from host | 16.7 MBytes/s (burst) |
| Sustained read | up to 10 MBytes/s |
| Sustained write | up to 10 MBytes/s |

## Reliability

| Parameter | Value |
|---|---|
| Data write/erase endurance | 2 million cycles min. |
| Data reliability | 1 in $10^{14}$ bits, read |
| Data retention | 10 years |

## Environmental Characteristics

| Parameter | Value |
|---|---|
| Shock | 1K G, half-sine, 0.330 ms to 0.750 ms<br>(per MIL-STD-202G Method 213B, Condition A) |
| Vibration | 15 G 10Hz-2KHz<br>(per MIL-STD-202G Method 204D 20 min/sweep, 12 sweeps/axis) |
| Humidity | 85°C 95% RH, 5.5V, 500 hrs |

## CHS Parameters

| Capacity | C | H | S |
|---|---|---|---|
| 128MB | 980 | 8 | 32 |
| 256MB | 980 | 16 | 32 |
| 512 MB | 993 | 16 | 63 |
| 1GB | 1986 | 16 | 63 |
| 2GB | 3970 | 16 | 63 |
| 3GB | 6022 | 16 | 63 |
| 4GB | 7964 | 16 | 63 |
| 5GB | 10038 | 16 | 63 |
| 6GB | 12046 | 16 | 63 |
| 7GB | 14054 | 16 | 63 |
| 8GB | 16062 | 16 | 63 |
| C = cylinders, H = heads, S = sectors/track | | | |

## DC Characteristics-1

(Ta=0 to 70°C for commercial temperature parts, -40 to 85°C for industrial temperature parts; VCC=3.3V +5% or -3.6%)

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| VIL | Input LOW Voltage | -0.3 | +0.8 | V | |
| VIH | Input HIGH Voltage | 2.0 | VCC +0.3 | V | |
| VOL | Output LOW Voltage | | 0.45 | V | at 4mA |
| VOH | Output HIGH Voltage | 2.4 | | V | at 1mA |
| ICC | Current VCC=3.3V<br>Sleep mode<br>Operating Current | | <br>2<br>75* | <br>mA<br>mA | |
| ILI | Input Leakage Current | | 10 | µA | |
| ILO | Output Leakage Current | | 1 | µA | |
| CI/O | Input/output Capacitance | | 25 | pF | |

* The operating current is measured for the firmware with 2-way interleaving

## DC Characteristics-2

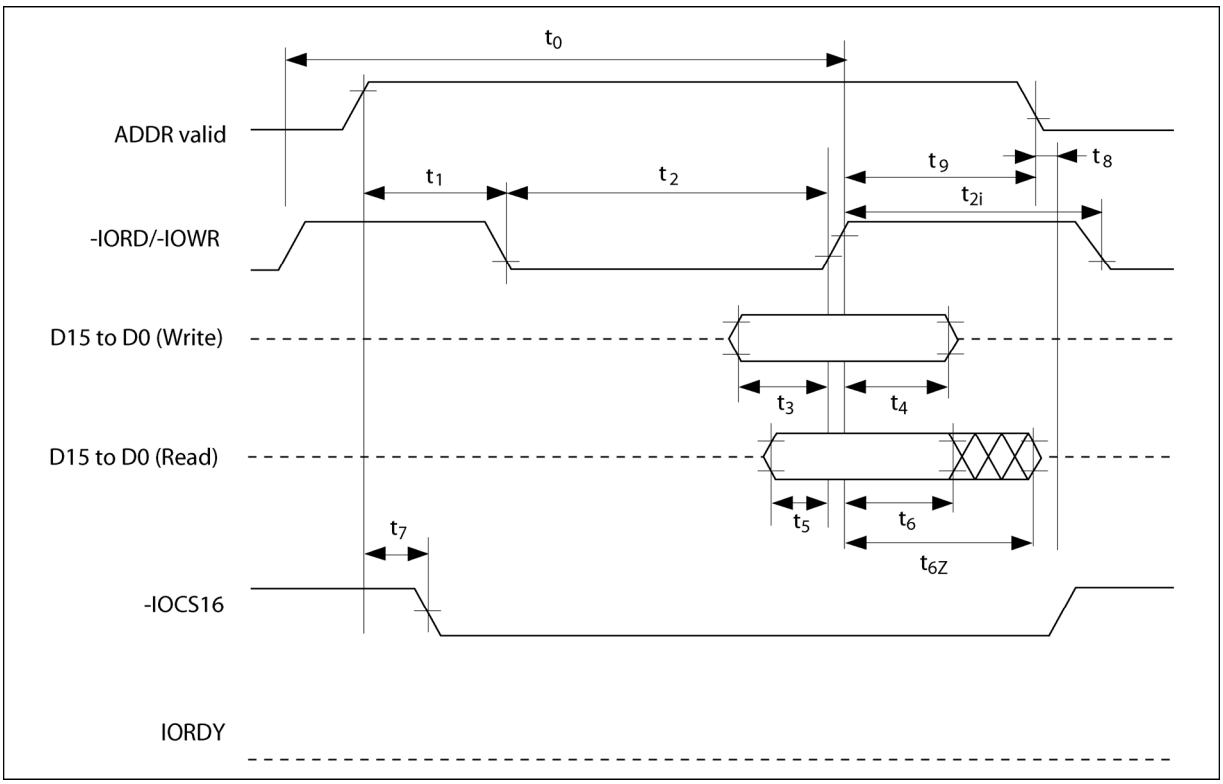
(Ta=0 to 70°C for commercial temperature parts, -40 to 85°C for industrial temperature parts; VCC=5V ±5%)

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| VIL | Input LOW Voltage | -0.3 | +0.8 | V | |
| VIH | Input HIGH Voltage | 2.0 | VCC+0.3 | V | |
| VOL | Output LOW Voltage | | 0.8 | V | at 4mA |
| VOH | Output HIGH Voltage | 2.4 | | V | at 1mA |
| ICC | Current, VCC=5.0V<br>Sleep mode<br>Operating mode | | <br>2<br>75* | <br>mA<br>mA | |
| ILI | Input Leakage Current | | 10 | µA | |
| ILO | Output Leakage Current | | 2 | µA | |
| CI/O | Input/output Capacitance | | 25 | pF | |

* The operating current is measured for the firmware with 2-way interleaving

## AC Characteristics

### True IDE Mode Access Read/Write Timings



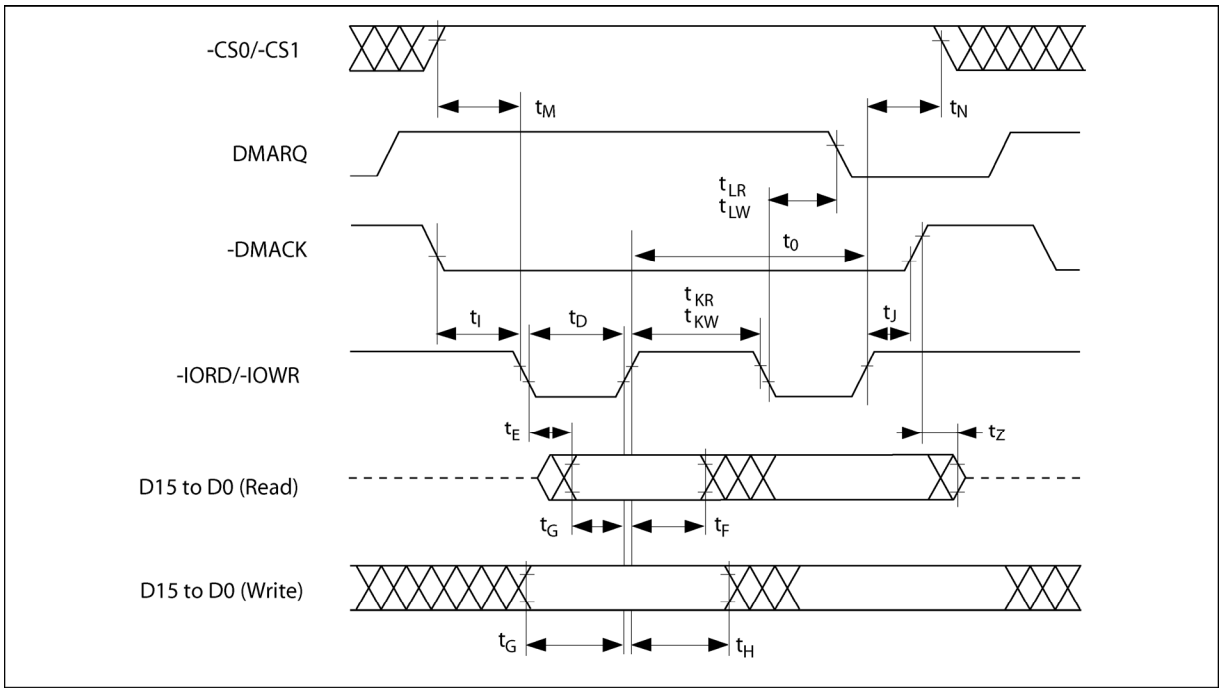
## AC Characteristics (*continued*)

### Multiword DMA Mode Access AC Characteristics for True IDE

| Parameter | Symbol | Mode 0 | Mode 1 | Mode 2 | Mode 3 | Mode 4 | Unit |
|---|---|---|---|---|---|---|---|
| Cycle time (min) | $t_0$ | 480 | 150 | 120 | 100 | 80 | ns |
| -IORD/-IOWR Asserted Pulse (min) | $t_D$ | 215 | 80 | 70 | 65 | 55 | ns |
| -IORD data access (max) | $t_E$ | 150 | 60 | 50 | 50 | 45 | ns |
| -IORD data hold (min) | $t_F$ | 5 | 5 | 5 | 5 | 5 | ns |
| -IORD/-IOWR data setup (min) | $t_G$ | 100 | 30 | 20 | 15 | 10 | ns |
| -IOWR data hold (min) | $t_H$ | 20 | 15 | 10 | 5 | 5 | ns |
| DMACK to – IORD/-IOWR setup (min) | $t_I$ | 0 | 0 | 0 | 0 | 0 | ns |
| -IORD/-IOWR to DMACK hold (min) | $t_J$ | 20 | 5 | 5 | 5 | 5 | ns |
| -IORD negated pulse width (max) | $t_{KR}$ | 50 | 50 | 25 | 25 | 20 | ns |
| -IOWR negated pulse width (min) | $t_{KW}$ | 215 | 50 | 25 | 25 | 20 | ns |
| -IORD to DMARQ delay (max) | $t_{LR}$ | 120 | 40 | 35 | 35 | 35 | ns |
| -IOWR to DMARQ delay (max) | $t_{LW}$ | 40 | 40 | 35 | 35 | 35 | ns |

## AC Characteristics (*continued*)

### Multiword DMA Mode Access Read/Write Timings



## Host Access Specification

### True IDE Mode

The drive is configured in a True IDE mode at power up. In the True IDE mode, the data register is accessed in word (16-bit) mode at power up. The card permits 8-bit accesses if the host issues a Set Feature Command to put the device in 8-bit mode.

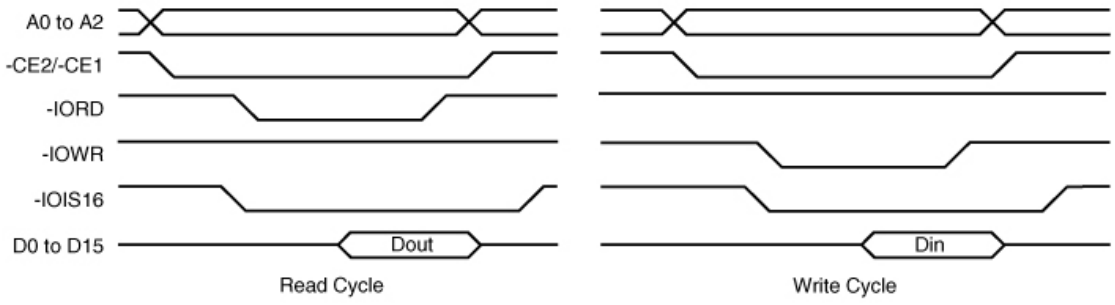
***True IDE Mode Read I/O Function***

| Mode | -CE2 | -CE1 | A0 to A2 | -IORD | -IOWR | D15 – D8 | D7 – D0 |
|---|---|---|---|---|---|---|---|
| Invalid Mode | L | L | x | x | x | High Z | High Z |
| Standby Mode | H | H | x | x | x | High Z | High Z |
| Data Register Access | H | L | 0 | L | H | Odd Byte | Even Byte |
| Alternate Status Access | L | H | 6h | L | H | High Z | Status Out |
| Other Task File Access | H | L | 1 - 7h | L | H | High Z | Data |
| **Legend:** *x* = L or H | | | | | | | |

***True IDE Write I/O Function***

| Mode | -CE2 | -CE1 | A0 to A2 | -IORD | -IOWR | D15 – D8 | D7 – D0 |
|---|---|---|---|---|---|---|---|
| Invalid Mode | L | L | x | x | x | Don't Care | Don't Care |
| Standby Mode | H | H | x | x | x | Don't Care | Don't Care |
| Data Register Access | H | L | 0 | H | L | Odd Byte | Even Byte |
| Alternate Status Access | L | H | 6h | H | L | Don't Care | Control In |
| Other Task File Access | H | L | 1-7h | H | L | Don't Care | Data |
| **Legend:** *x* = L or H | | | | | | | |

***True IDE Mode I/O Access Timing Example***



## Task File Register Specification

These registers are used for reading and writing data to the card.

### True IDE Mode I/O Map

| -CE2 | -CE1 | A2 | A1 | A0 | -IORD=0 | IOWR=0 |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | Data register | Data register |
| 1 | 0 | 0 | 0 | 1 | Error register | Feature register |
| 1 | 0 | 0 | 1 | 0 | Sector Count register | Sector Count register |
| 1 | 0 | 0 | 1 | 1 | Sector No. register | Sector No. register |
| 1 | 0 | 1 | 0 | 0 | Cylinder Low register | Cylinder Low register |
| 1 | 0 | 1 | 0 | 1 | Cylinder High register | Cylinder High register |
| 1 | 0 | 1 | 1 | 0 | Drive Head register | Drive Head register |
| 1 | 0 | 1 | 1 | 1 | Status register | Command register |
| 0 | 1 | 1 | 1 | 0 | Alt Status register | Device Ctl register |
| 0 | 1 | 1 | 1 | 1 | Drive Address register | Reserved |

### Data Register

The Data Register is a 16-bit read/write register used for transferring data between the card and the host. This register can be accessed in word mode and byte mode.

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Field | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

## Error Register

The Error Register is a read-only register that is used for analyzing an error. This register is valid when the BSY bit in the Status register and Alternate Status register are set to “0” (Ready).

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | BBK | UNC | 0 | IDNF | 0 | ABRT | 0 | AMNF |
| R/W | R | R | R | R | R | R | R | R |

| Bits | Name | R/W | Function |
|---|---|---|---|
| 7 | Bad Block Detected (BBK) | R | This bit is set when a bad block is detected in requested ID field—not supported |
| 6 | Data ECC Error (UNC) | R | This bit is set when an Uncorrectable error has occurred when reading the card. |
| 4 | ID Not Found (IDNF) | R | The requested sector ID is in error or cannot be found. |
| 2 | Aborted Command (ABRT) | R | Drive status error or aborted invalid command |
| 0 | Address Mark Not Found (AMNF) | R | This bit is set in case of a general error. |

| Diagnostic Code | Function |
|---|---|
| 01h | No error detected |
| 02h | Formatting error |
| 03h | Sector buffer error |
| 04h | ECC error |
| 05h | Microprocessor error |
| 8xh | Drive 1 failed (not used) |

## Feature Register

This write-only register provides information regarding the features of the card which the host wishes to utilize. See details under the Set Features command on page 27.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Feature Byte | | | | | | | |
| R/W | W | W | W | W | W | W | W | W |

## Sector Count Register

This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the card. If the value in the register is 0, a count of 256 sectors is indicated.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Sector Count Byte | | | | | | | |

## Sector Number Register

When the LBA bit in the Drive/Head register is 0, this register contains the starting sector number for any media access. When the LBA bit is set to 1, this register contains bits 7:0 of the LBA for any media access.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Sector Number Byte or bits 7:0 of the LBA | | | | | | | |

## Cylinder Low Register

In CHS mode (LBA=0), this register contains the low-order bits of the starting cylinder address. In LBA mode, it contains bits 15:8 of the LBA.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Cylinder Low Byte or bits 15:8 of the LBA | | | | | | | |

## Cylinder High Register

In CHS mode (LBA=0), this register contains the high-order bits of the starting cylinder address. In LBA mode, it contains bits 23:16 of the LBA.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Cylinder High Byte or bits 23:16 of the LBA | | | | | | | |

## Drive/Head Register

This register selects the device address translation (CHS or LBA) and provides head address (CHS) or high-order address bits 27:24 for LBA.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | 1 | LBA | 1 | DRV | Head No. or bits 27:24 of the LBA | | | |

| Bits | Name | Function |
|---|---|---|
| 7 | 1 | This bit is set to 1. |
| 6 | LBA | LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address (LBA) mode. When LBA=0, CHS mode is selected.<br>1 = LBA mode is selected. In LBA mode, the Logical Block Address is interrupted as follows:<br>LBA07-LBA00: Sector Number Register D7-D0<br>LBA15-LBA08: Cylinder Low Register D7-D0<br>LBA23-LBA16: Cylinder High Register D7-D0<br>LBA27-LBA24: Drive/Head Register bits HS3-HS0 |
| 5 | 1 | This bit is set to 1. |
| 4 | DRV | This bit is used for selecting the Master (Card 0) and Slave (Card 1) in Master/Slave organization. The card is set to be Card 0 or 1 by using DRV# of the Socket and Copy register. |
| 3 - 0 | Head Number (HS3 - HS0) | These bits select the Head number. Bit 3 is MSB. In LBA mode, these bits represent the LBA address 27:24. |

## Status Register

This read-only register indicates status of a command execution. When the BSY bit is “0”, the other bits are valid; when the BSY bit is “1”, the other bits are not valid. When the register is read, the interrupt pin, -IREQ (INTRQ), is cleared.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | BSY | DRDY | DWF | DSC | DRQ | CORR | IDX | ERR |
| R/W | R | R | R | R | R | R | R | R |

| Bits | Name | R/W | Function |
|---|---|---|---|
| 7 | Busy (BSY) | R | This bit is set when the card internal operation is executing. 1 = other bits in this register are invalid. |
| 6 | Drive ReadY (DRDY) | R | This bit and DSC bit are set to 1 = the card can receive the read and write or seek requests. 0 = the card prohibits these requests. On error, DRDY changes only after the host reads the Status Register. |
| 5 | Drive Write Fault (DWF) | R | This bit is set if a fault occurs during the write process. |
| 4 | Drive Seek Complete (DSC) | R | This bit is set when the requested sector was found. |
| 3 | Data Request (DRQ) | R | This bit is set when information can be transferred between the host and data register. |
| 2 | Corrected Data (CORR) | R | This bit is set when a correctable data error has occurred and the data has been corrected. |
| 1 | Index (IDX) | R | This bit is always set to 0. |
| 0 | Error (ERR) | R | This bit is set when the previous command has ended in some type of error. The error information is set in the Error register. |

## Alternate Status Register

This register is the same as the Status register, except that –IREQ (INTRQ) is not negated when data is read.

## Command Register

This write-only register is used for writing the command that executes the card’s operation. The command code is written in the command register after its parameters are written in the Task File during the card ready state. See details under the ATA Command Specifications on page 23.

## Device Control Register

This write-only register is used for controlling the interrupt request and issuing an ATA soft reset to the card.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | x | x | x | x | 1 | SRST | nIEN | 0 |
| R/W | W | W | W | W | W | W | W | W |

| Bits | Name | R/W | Function |
|---|---|---|---|
| 7 – 4 | X | W | Don't'Care |
| 3 | 1 | W | This bit is set to 1. |
| 2 | Software Reset (RST) | W | 1 = forces the card to perform an AT disk control soft reset operation. |
| 1 | Interrupt Enable (nIEN) | W | 0 = enables interrupts to the host (using the -IREQ tri-state pin). 1 (inactive) or drive is not selected = all pending interrupts (-IREQ in high-Z) are disabled. This bit is ignored in memory mode. |
| 0 | 0 | W | This bit is set to 0. |

## Drive Address Register

This read-only register is used for confirming the card's status. This register is provided for compatibility with the AT disk drive interface and it is not recommended that this register be mapped into the host's I/O space because of potential conflicts on bit 7.

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | High-Z | nWTG | nHS3 | nHS2 | nHS1 | nHS0 | nDS1 | nDS0 |
| R/W | R | R | R | R | R | R | R | R |

| Bits | Name | R/W | Function |
|---|---|---|---|
| 7 | High-Z | R | This bit is not used. |
| 6 | nWTG (WriTing Gate) | R | This bit is not used. |
| 5 - 2 | nHS3-0 (Head Select 3-0) | R | These bits are the negative value of the Head Select bits (bit 3 to 0) in the Drive/Head register |
| 1 | nDS1 (Drive Select 1) | R | 0 = drive 1 is active and selected. |
| 0 | nDS0 (Drive Select 0) | R | 0 = drive 0 is active and selected. |

## ATA Command Specifications

| No. | Command Set | Code | FR | SC | SN | CY | DR | HD | LBA |
|---|---|---|---|---|---|---|---|---|---|
| 1 | Check Power Mode | E5h or 98h | — | Y | — | — | Y | — | — |
| 2 | Execute Drive Diagnostic | 90h | — | — | — | — | Y** | — | — |
| 3 | Erase Sector(s) | C0h | — | Y | Y | Y | Y | Y | Y |
| 4 | Format Track | 50h | — | Y | — | Y | Y | Y | Y |
| 5 | Identify Drive | ECh | Y | — | — | — | Y | — | — |
| 6 | Idle | E3h or 97h | — | Y | — | — | Y | — | — |
| 7 | Idle Immediate | E1h or 95h | — | — | — | — | Y | — | — |
| 8 | Initialize Drive Parameters | 91h | — | Y | — | — | Y | Y | — |
| 9 | NOP | 00h | — | — | — | — | — | Y | — |
| 10 | Read Buffer | E4h | — | — | — | — | Y | — | — |
| 11 | Read DMA | C8h | — | Y | Y | Y | Y | Y | Y |
| 12 | Read Multiple | C4h | — | Y | Y | Y | Y | Y | Y |
| 13 | Read Long Sector | 22h or 23h | — | — | Y | Y | Y | Y | Y |
| 14 | Read Sector(s) | 20h or 21h | — | Y | Y | Y | Y | Y | Y |
| 15 | Read Verify Sector(s) | 40h or 41h | — | Y | Y | Y | Y | Y | Y |
| 16 | Recalibrate | 1Xh | — | — | — | — | Y | — | — |
| 17 | Request Sense | 03h | — | — | — | — | Y | — | — |
| 18 | Seek | 7Xh | — | — | Y | Y | Y | Y | Y |
| 19 | Set Features | EFh | — | Y | Y | Y | Y | Y | — |
| 20 | Set Multiple Mode | C6h | — | Y | — | — | Y | — | — |
| 21 | Set Sleep Mode | E6h or 99h | — | — | — | — | Y | — | — |
| 22 | Stand By | E2h or 96h | — | Y | — | — | Y | — | — |
| 23 | Stand By Immediate | E0h or 94h | — | — | — | — | Y | — | — |
| 24 | Translate Sector | 87h | — | Y | Y | Y | Y | Y | Y |
| 25 | Wear Level | F5h | — | — | — | — | Y | Y | — |
| 26 | Write Buffer | E8h | — | — | — | — | Y | — | — |
| 27 | Write DMA | CAh | — | Y | Y | Y | Y | Y | Y |
| 28 | Write Long Sector | 32h or 33h | — | Y | Y | Y | Y | Y | Y |
| 29 | Write Multiple | C5h | — | Y | Y | Y | Y | Y | Y |
| 30 | Write Multiple w/o Erase | CDh | — | Y | Y | Y | Y | Y | Y |
| 31 | Write Sector(s) | 30h or 31h | — | Y | Y | Y | Y | Y | Y |
| 32 | Write Sector(s) w/o Erase | 38h | — | Y | Y | Y | Y | Y | Y |
| 33 | Write Verify | 3Ch | — | Y | Y | Y | Y | Y | Y |

Legend:
FR = Features register
SC = Sector Count register (00h to FFh)
SN = Sector Number register (01h to 20h)
CY = Cylinder registers
LBA = Logical Block Address Mode Supported
Y = Valid bit , "—" = N/A
** Address to drive 0. Both drives execute command.
DR = Drive bit of Drive/Head register
HD = Head no. (0 to 3) of Drive/Head register

## Check Power Mode (code: E5h or 98h)

This command checks the power mode.

## Execute Drive Diagnostic (code: 90h)

This command performs the internal diagnostic tests implemented by the card. See the Error Register on page 18 for diagnostic codes.

## Erase Sector(s) (code: C0h)

This command is used to pre-erase and condition data sectors in advance.

## Format Track (code: 50h)

This command writes the desired head and cylinder of the selected drive with a vender unique data pattern (typically 00h or FFh). This card accepts a sector buffer of data from the host to follow the command with the same protocol as the Write Sector Command although the information in the buffer is not used.

## Identify Drive (code: ECh)

This command lets the host receive parameter information from the card (see the following table).

| Word Address | Data | Total Bytes | Description |
|---|---|---|---|
| 0 | 044AH | 2 | Value fixed by CFA |
| 1 | XXXXH | 2 | Default number of cylinders |
| 2 | 0000H | 2 | Reserved |
| 3 | 00XXH | 2 | Default number of heads |
| 4 | XXXXH | 2 | Do not use this word. Before retirement, was number of unformatted bytes per track |
| 5 | XXXXH | 2 | Do not use this word. Before retirement, was number of unformatted bytes per sector |
| 6 | XXXXH | 2 | Default number of sectors per track |
| 7 - 8 | XXXXH | 4 | Number of sectors per card (word 7 = MSW, word 8 = LSW) |
| 9 | 0000H | 2 | Reserved |
| 10 - 19 | XXXXH | 20 | Serial Number (see table next page for definition) |
| 20 | XXXXH | 2 | Do not use this word. Before retirement, was buffer type |
| 21 | XXXXH | 2 | Do not use this word. Before retirement, was buffer size in 512 byte increments |
| 22 | 0004H | 2 | # of ECC bytes passed on Read/Write Long commands |
| 23 - 46 | XXXXH | 48 | Firmware revision and model number in ASCII (see table on the next page) |
| 47 | 0001H | 2 | Maximum of 1 sector on Read/Write Multiple command |
| 48 | 0000H | 2 | Double Word not supported |
| 49 | 0300H | 2 | DMA supported, LBA supported |
| 50 | 0000H | 2 | Reserved |
| 51 | 0200H | 2 | PIO data transfer cycle timing mode |
| 52 | 0000H | 2 | Single word DMA data transfer cycle timing mode (not supported) |
| 53 | 0003h | 2 | Words 54 - 58 and 64 - 70 are valid |
| 54 | XXXXH | 2 | Number of Current Cylinders |
| 55 | XXXXH | 2 | Number of Current Heads |
| 56 | XXXXH | 2 | Number of Current Sectors Per Track |
| 57 | XXXXH | 2 | LSW of the Current Capacity in Sectors |
| 58 | XXXXH | 2 | MSW of the Current Capacity in Sectors |
| 59 | 010XH | 2 | Current Setting for Block Count=1 for R/W Multiple commands |
| 60 - 61 | XXXXH | 4 | Total number of sectors addressable in LBA Mode |
| 62 | 0000H | 2 | Single word DMA transfer not supported |

| | | | |
|---|---|---|---|
| 63 | 0407H | 2 | Multiword DMA modes supported |
| 64 | 0003H | 2 | Advanced PIO modes supported (modes 3 and 4) |
| 65 | 0078H | 2 | Minimum multiword DMA transfer cycle time per word (ns) |
| 66 | 0078H | 2 | Recommended multiword DMA transfer cycle time per word (ns) |
| 67 | 0078H | 2 | Minimum PIO transfer without flow control |
| 68 | 0078H | 2 | Minimum PIO transfer with IORDY flow control |
| 69 - 255 | 0000H | 388 | Reserved |
| XXXXH = These values depend on the specific card. | | | |

| Serial Number Format (typical): Words 10-19 | | | | | |
|---|---|---|---|---|---|
| SimpleTech Proprietary | Yr | Day | Hr | Min | Sec |
| STI_J13C0 | 04 | 224 | 09 | 27 | 50 |
| Firmware Revision: Words 23-26<br><br>mm/dd/yy | | | | | |
| Model Number: Words 27-46<br>STI Flash X.Y.Z | | | | | |

## Idle (code: E3h or 97h)

This command causes the card to set BSY, enter the Idle mode, clear BSY, and generate an interrupt. If the sector count is non-zero, automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.

## Idle Immediate (code: E1h or 95h)

This command causes the card to set BSY, enter the Idle (Read) mode, clear BSY, and generate an interrupt.

## Initialize Drive Parameters (code: 91h)

This command enables the host to set the number of sectors per track and the number of heads per cylinder.

## Read Buffer (code: E4h)

This command enables the host to read the current contents of the card's sector buffer.

## Read DMA (code: C8h)

This command is the sector read command used for Multiword DMA transfer.

## Read Multiple (code: C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

## Read Long Sector (code: 22h or 23h)

This command performs similarly to the Read Sector(s) command except that it returns 516 bytes of data instead of 512 bytes.

## Read Sector(s) (code: 20h or 21h)

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

## Read Verify Sector(s) (code: 40h or 41h)

This command verifies one or more sectors on the card by transferring data from the flash media to the data buffer in the card and verifying that the ECC is correct. This commandis identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

## Recalibrate (code: 1Xh)

The card performs only the interface timing and register operations. When this command is issued, the card sets BSY and waits for an appropriate length of time, after which it clears BSY and issues an interrupt. When this command ends normally, the card is initialized.

## Request Sense (code: 03h)

This command requests an extended error code after a command ends with an error (see the following table).

| Code | Description |
|---|---|
| 00H | No error detected |
| 01H | Self test OK (no error) |
| 09H | Miscellaneous Error - N/A |
| 20H | Invalid Command |
| 21H | Invalid Address (requested Head or Sector invalid) |
| 2FH | Address Overflow (address too large) |
| 35H, 36H | Supply or generate Voltage Out of Tolerance |
| 11H | Uncorrectable ECC Error |
| 18H | Correctable ECC Error - N/A |
| 05H, 30H-34H, 37H, 3EH | Self Test Diagnostic Failed |
| 10H, 14H | ID Not Found - N/A |
| 3AH | Spare Sectors Exhausted |
| 1FH | Data Transfer Error / Aborted Command |
| 0CH, 38H, 3BH, 3CH, 3FH | Corrupted Media Format - N/A |
| 03H | Write / Erase Failed - N/A |
| 22H | Power Level 1 Disabled |

### Seek (code: 7Xh)

This command is effectively a NOP command to the card although it does perform a range check.

### Set Features (code: EFh)

This command is used by the host to establish or select certain features.

| Code | Description |
|---|---|
| 01H | Enable 8-bit data transfers. |
| 55H | Disable Read Look Ahead. |
| 66H | Disable Power on Reset (POR) establishment of defaults at Soft Reset. |
| 81H | Disable 8-bit data transfers. |
| BBH | Four bytes of data apply on Read/Write Long commands. |
| CCH | Enable Power on Reset (POR) establishment of default at Soft Reset. |

### Set Multiple Mode (code: C6h)

This command enables the card to perform multiple read and write operations and establishes the block count for these commands.

### Set Sleep Mode (code: E6h or 99h)

This is the only command that allows the host to set the card into Sleep mode. When the card is set to sleep mode, the card clears the BSY line and issues an interrupt. The card enters sleep mode and the only method to make the card active again (back to normal operation) is by performing a hardware reset or a software reset.

### Stand By (code: E2h or 96h)

This command is sets the card in Standby mode. If the Sector Count Register is a value other than 0H, an Auto Power Down is enabled and when the card returns to the idle mode, the timer starts a countdown. The time is set in the Sector Count Register.

### Stand By Immediate (code: E0h or 94h)

This command causes the card to set BSY, enter the Standby mode, clear BSY and return the interrupt immediately.

### Translate Sector (code: 87h)

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. This command is not supported.

### Wear Level (code: F5h)

This command is effectively a NOP command and only implemented for backward compatibility. The Sector Count Register will always be returned with an 00h indicating Wear Level is not needed.

### Write Buffer (code: E8h)

This command enables the host to overwrite the contents of the card's sector buffer with any data pattern desired.

### Write DMA (code: CAh)

This command is the sector write command used for Multiword DMA transfer.

### Write Long Sector (code: 32h or 33h)

This command is provided for compatibility purposes and is similar to the Write Sector(s) command except that it writes 516 bytes instead of 512 bytes.

### Write Multiple (code: C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

### Write Multiple Without Erase (code: CDh)

This command is similar to the Write Multiple command, except that an implied erase before the write operation is not performed.

***Note***: Before using this command, it is required to erase the repective sectors using the Erase Sectors command.

### Write Sector(s) (code: 30h or 31h)

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

### Write Sector(s) Without Erase (code: 38h)

This command is similar to the Write Sector(s) command, except that an implied erase before the write operation is not performed.

***Note***: Before using this command, it is required to erase the repective sectors using the Erase Sectors command.

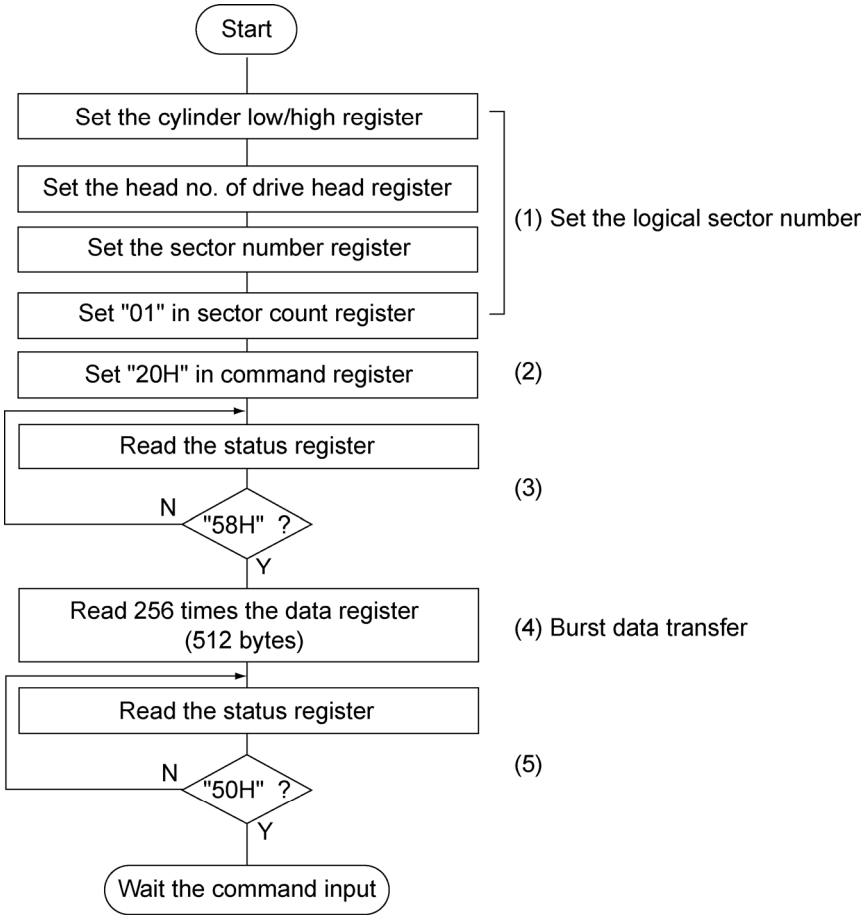
### Write Verify (code: 3Ch)

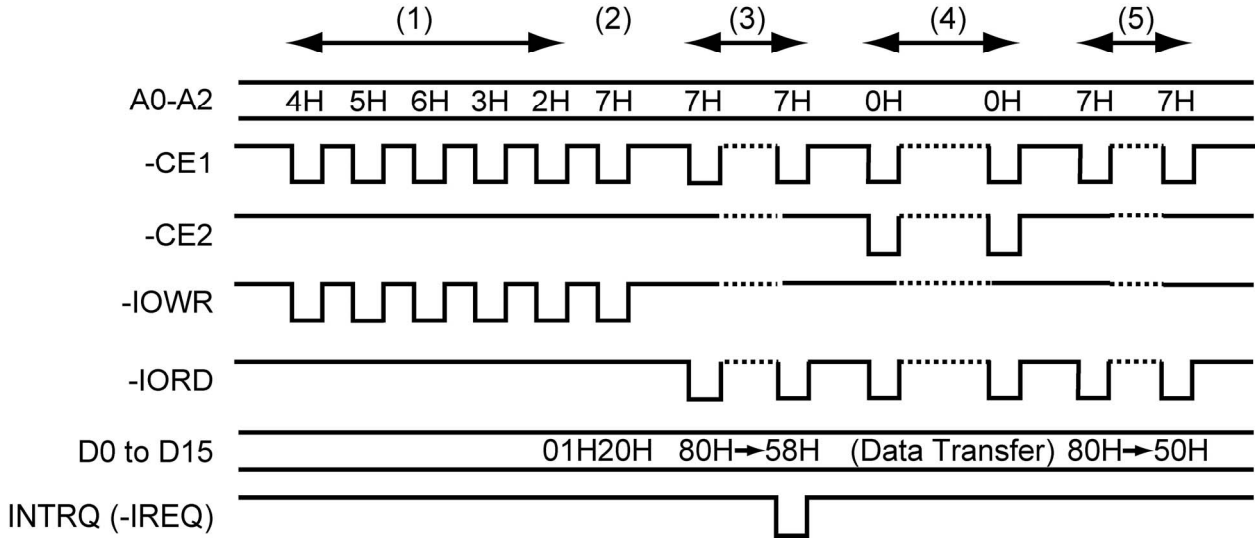
This command is similar to the Write Sector(s) command except each sector is verified immediately after being written.

## Sector Transfer Protocol

### Sector Read

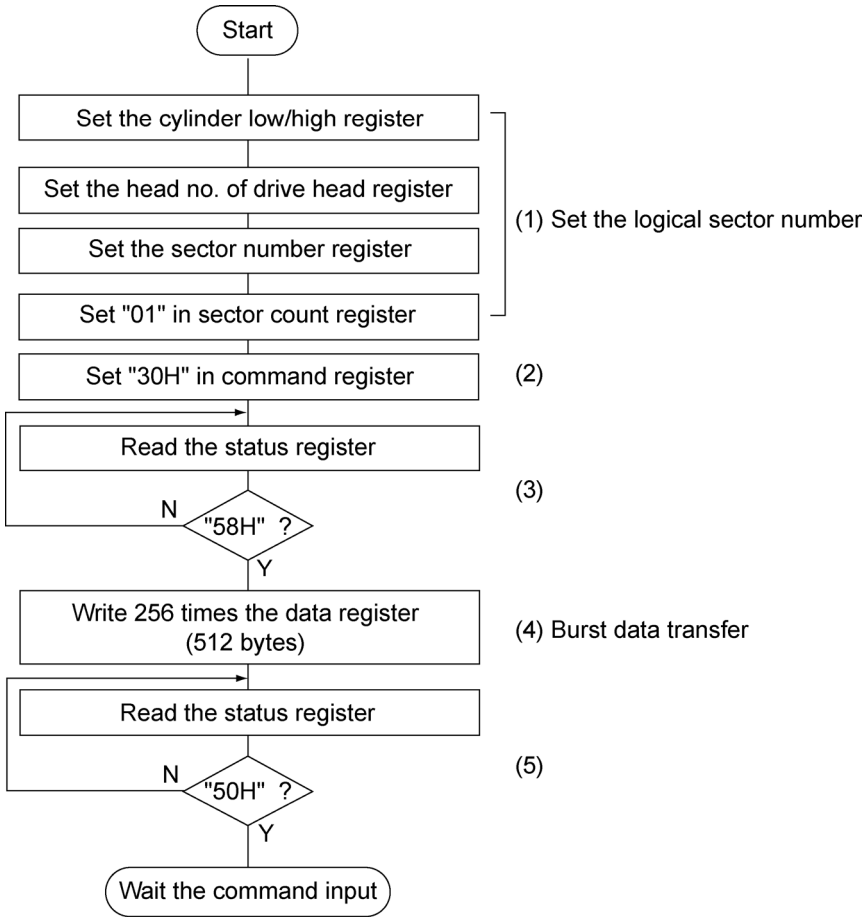
One sector read procedure after the card is configured to I/O interface is shown in the following figures.

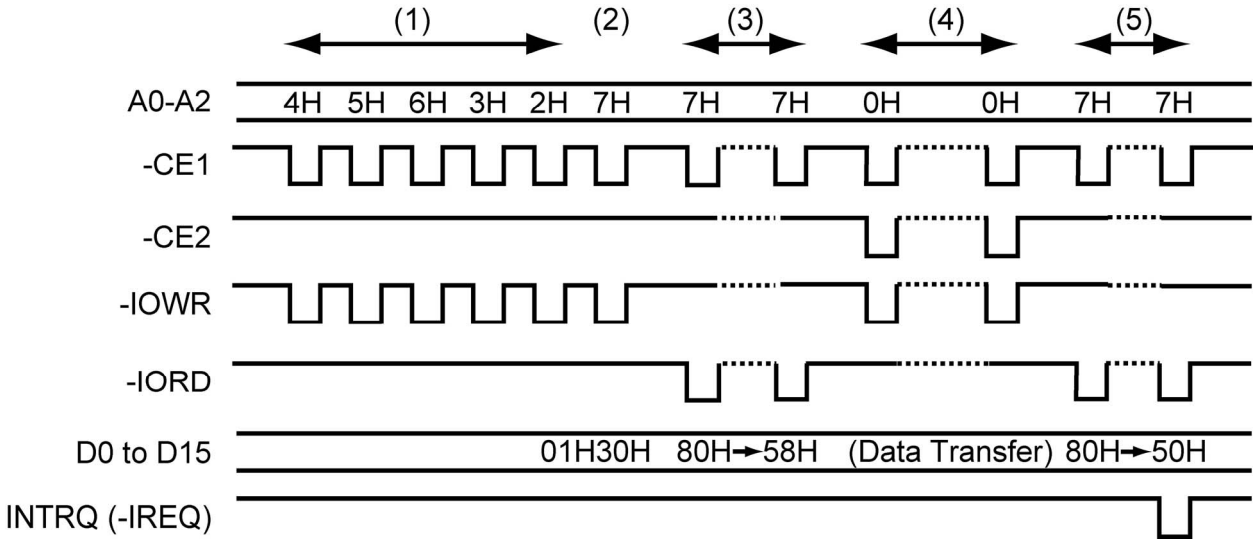


## Sector Write

One sector write procedure after the card is configured to I/O interface is shown in the following figures.



## Revision History

| *Revision* | *Date* | *Description* |
|---|---|---|
| -101 | 8/1/06 | Initial release. |
| -102 | 8/4/06 | Phantom part number changed from SLFLDxxxxM1(T2)U(I) to SLFLD25-xxx(M/G)M1(T2)U(I). |

## Index